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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/692,297	10/19/2000	Peter Ballam	S1022/8544	4272

7590 04/07/2004

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EXAMINER	
BARNES, CRYSTAL J	

ART UNIT	PAPER NUMBER
2121	6

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/692,297	BALLAM, PETER	
	Examiner	Art Unit	
	Crystal J. Barnes	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is an initial Office Action upon examination of the above-identified application on the merits. Claims 1-9 are pending in this application.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.

(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)

(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(f) BRIEF SUMMARY OF THE INVENTION.

(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(h) DETAILED DESCRIPTION OF THE INVENTION.

(i) CLAIM OR CLAIMS (commencing on a separate sheet).

(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

4. Claims 1 and 7 are objected to because of the following informalities: Since "between" is used to associate two items, join the two items with "and" as in "between an input signal and an output signal". It is incorrect to use "or".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Regarding claim 1, the phrase "a bi-directional pin of said model applying signals to said pin" on lines 4-5 of the claim renders the claim indefinite because it is unclear how "a bi-directional pin" can apply signals to itself.

8. Regarding claims 1 and 7, the phrase "comparing the drive strength" on line 8 of the claim renders the claim indefinite because it is unclear whether "the drive strength" refers to the applied signal or the driven signal or both.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1 and 2 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 4 and 5 of USPN 6,560,757 B1 to Ballam in view of USPN 6,363,509 B1 to Parulkar et al.

The Ballam reference claims a method of verifying an output from an analog simulation model of a hardware circuit by applying a preselected voltage (signals) to an input pin (bi-directional pin) of an analog simulation model (model); driving the pin (bi-directional pin) with the selected test voltage (applied signal) for the output pin (bi-directional pin) at a drive strength (reduced drive strength) which is weaker than a drive strength of the expected output voltage (drive signal) on the output pin (bi-directional pin); comparing the measured output voltage and the expected output voltage (drive strength); and responsive to the comparison (comparing), providing a verifying output (output) if the measured and expected output voltages (drive strength of applied signal and drive signal) are not in contradiction (input/output). The Ballam reference does not expressly claim a method of

distinguishing between an input and output signal on a bi-directional pin of a model of a hardware circuit.

The Parulkar et al. reference discloses the ATE induces drive events on certain pins (input pins and bi-directional pins acting as inputs at that time) ... comparators are used to strobe certain pins (output pins and bi-directional pins acting as outputs at the time) and compare the strobed values to expected responses of the integrated circuit under those conditions (see column 5 lines 58-67). The Parulkar et al. reference also discloses the I/O cell information is used to identify the pins within the simulation model which are either bi-directional or output pins (see column 8 lines 9-16). The test patterns are preferably contained in a file as a list of applied values to the inputs and bi-directional pins acting as inputs, and expected values from the outputs and the bi-directional pins acting as outputs (see column 14 lines 27-30).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of verification taught by the Ballam reference with the techniques for functionally testing integrated circuit chips taught by the Parulkar et al. reference to verify the design of a simulation model of an electronic system.

One of ordinary skill in the art would have been motivated to verify the design of a simulation model of an electronic system so that integrated circuit chips can be tested more thoroughly and cost effectively.

11. Claims 3-5 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 4 and 5 of USPN 6,560,757 B1 to Ballam in view of USPN 6,363,509 B1 to Parulkar et al.

The Ballam reference claims a method of verifying an output from an analog simulation model of a hardware circuit by applying a preselected voltage (signals) to an input pin (bi-directional pin) of an analog simulation model (model); driving the pin (bi-directional pin) with the selected test voltage (applied signal) for the output pin (bi-directional pin) at a drive strength (reduced drive strength) which is weaker than a drive strength of the expected output voltage (drive signal) on the output pin (bi-directional pin); comparing the measured output voltage and the expected output voltage (drive strength); and responsive to the comparison (comparing), providing a verifying output (output) if the measured and expected output voltages (drive strength of applied signal and drive signal) are not in contradiction (input/output). The Ballam reference does not expressly claim a method of

distinguishing between an input and output signal on a bi-directional pin of a HDL digital model of a hardware circuit, wherein the HDL digital model utilizes the standard HDL values and a strong signal on the bi-directional pin is replaced by a Z.

The Parulkar et al. reference discloses Verilog HDL is an example of a design descriptive language that supports simulation at various levels of chip design (see column 1 lines 18-22). The Parulkar et al. reference also discloses the simulation model 308 is a model built in a modeling and simulation software environment such as that provided by Verilog (see column 6 lines 35-37). The output data from the simulation tool 314 consists of logic values of I/O pins and control signals (see column 9 lines 15-25). Hence, the expected response for that pin ... should be 'Z' (high-impedance) ... interprets the '0' or '1' ... as 'Z' ... (see column 14 lines 21-25). A "0" logic value for a bi-directional pin implies that a logic "0" is driven in (input mode), while a "L" value ... implies that the pin is in the output mode and the expected response is a logic "0" (see column 14 lines 49-55). In addition ... "z" means high impedance ... (see column 14 lines 56-57).

The examiner interprets the simulated value of "0" or "1" as output of a digital model.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of verification taught by the Ballam reference with the techniques for functionally testing integrated circuit chips taught by the Parulkar et al. reference to verify the design of a digital simulation model of an electronic system.

One of ordinary skill in the art would have been motivated to verify the design of a digital simulation model of an electronic system so that integrated circuit chips can be tested more thoroughly and cost effectively.

12. Claim 6 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 of USPN 6,560,757 B1 to Ballam in view of USPN 6,363,509 B1 to Parulkar et al.

The Ballam reference claims a method of verifying an output from an analog simulation model of a hardware circuit by applying a preselected voltage (signals) to an input pin (bi-directional pin) of an analog simulation model (model); an output pin (bi-directional pin) is driven with a high voltage (drive strength greater); subsequently comparing the measured output voltage and the expected output voltage (drive strength); and responsive to the comparison (comparing), providing a

verifying output (output) if the measured and expected output voltages (drive strength of applied signal and drive signal) are not in contradiction (input/output). The Ballam reference does not expressly claim a method of distinguishing between an input and output signal on a bi-directional pin of a model of a hardware circuit.

The Parulkar et al. reference discloses the ATE induces drive events on certain pins (input pins and bi-directional pins acting as inputs at that time) ... comparators are used to strobe certain pins (output pins and bi-directional pins acting as outputs at the time) and compare the strobed values to expected responses of the integrated circuit under those conditions (see column 5 lines 58-67). The Parulkar et al. reference also discloses the I/O cell information is used to identify the pins within the simulation model which are either bi-directional or output pins (see column 8 lines 9-16). The test patterns are preferably contained in a file as a list of applied values to the inputs and bi-directional pins acting as inputs, and expected values from the outputs and the bi-directional pins acting as outputs (see column 14 lines 27-30).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of verification taught by the Ballam reference with the techniques for functionally testing integrated circuit

chips taught by the Parulkar et al. reference to verify the design of a simulation model of an electronic system.

One of ordinary skill in the art would have been motivated to verify the design of a simulation model of an electronic system so that integrated circuit chips can be tested more thoroughly and cost effectively.

13. Claim 7 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 12, 20 and 21 of USPN 6,560,757 B1 to Ballam in view of USPN 6,363,509 B1 to Parulkar et al.

The Ballam reference discloses a system for verifying an output from an analog simulation model of a hardware circuit by applying a preselected voltage (signals) to an input pin (bi-directional pin) of an analog simulation model (model); driving the pin (bi-directional pin) with the selected test voltage (applied signal) for the output pin (bi-directional pin) at a drive strength (reduced drive strength) which is weaker than a drive strength of the expected output voltage (drive signal) on the output pin (bi-directional pin); comparing the measured output voltage and the expected output voltage (drive strength); and responsive to the comparison (comparing), providing a verifying output (output) if the measured and expected

output voltages (drive strength of applied signal and drive signal) are not in contradiction (input/output). The Ballam reference does not expressly claim a method of distinguishing between an input and output signal on a bi-directional pin of a model of a hardware circuit.

The Parulkar et al. reference discloses the ATE induces drive events on certain pins (input pins and bi-directional pins acting as inputs at that time) ... comparators are used to strobe certain pins (output pins and bi-directional pins acting as outputs at the time) and compare the strobed values to expected responses of the integrated circuit under those conditions (see column 5 lines 58-67). The Parulkar et al. reference also discloses the I/O cell information is used to identify the pins within the simulation model which are either bi-directional or output pins (see column 8 lines 9-16). The test patterns are preferably contained in a file as a list of applied values to the inputs and bi-directional pins acting as inputs, and expected values from the outputs and the bi-directional pins acting as outputs (see column 14 lines 27-30).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of verification taught by the Ballam reference with the techniques for functionally testing integrated circuit

chips taught by the Parulkar et al. reference to verify the design of a simulation model of an electronic system.

One of ordinary skill in the art would have been motivated to verify the design of a simulation model of an electronic system so that integrated circuit chips can be tested more thoroughly and cost effectively.

14. Claim 8 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 10 of USPN 6,560,757 B1 to Ballam in view of USPN 6,363,509 B1 to Parulkar et al. as applied to claim 7 above.

15. Claim 9 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of USPN 6,560,757 B1 to Ballam in view of USPN 6,363,509 B1 to Parulkar et al. as applied to claim 7 above.

Conclusion

16. No claims are allowed.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to evaluating circuit designs in general:

USPN 6,499,125 B1 to Ohta et al.

USPN 6,370,493 B1 to Knapp et al.

USPN 6,353,915 B1 to Deal et al.

USPN 6,279,146 B1 to Evans et al.

JPPN 55-82972 A to NAKAMAE

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Crystal J. Barnes whose telephone number is 703.306.5448. The examiner can normally be reached on Monday-Friday alternate Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anil Khatri can be reached on 703.305.0282. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cjb
2 April 2004

EMANUEL TODD VOELTZ
PRIMARY EXAMINER